REMARKS

Claims 1-12 are pending in the application. Claims 1, 6, and 10 have been amended by the present amendment. The amendments are fully supported by the specification as originally filed.

Applicants' invention is directed to a tape carrier package structure which accommodates a semiconductor chip in a device hole of a tape carrier (such as TAB tape) and connects the chip to the tape carrier by inner leads. A plurality of I/O pads are formed along sides of the chip, and a plurality of dummy pads are arranged on the sides at positions (including corners) that are free of the I/O pads, where the dummy pads are spaced at the same pitch as the I/O pads. As a result, the sides of the chip are full of the plurality of equally spaced I/O pads and dummy pads.

As recited in independent claims 1, 6, and 10, the inner leads include a group of I/O leads which are bonded between the I/O pads and sides of the tape carrier around the device hole. A group of dummy leads are bonded between the dummy pads and corners of the tape carrier around the device hole. The dummy leads are spaced at substantially the same pitch as the I/O leads. The inner leads provide firm support to the chip and hold the chip in position with respect to the tape carrier, thereby enhancing the mechanical strength of the package structure.

The above-described semiconductor package structure can yield significant benefits. By providing the claimed arrangement of equally spaced pads and leads, during the potting process, the encapsulation material will be more evenly distributed on the semiconductor chip, thereby preventing the occurrence of voids or popcorn effect in the resulting encapsulation body.

Claims 1-12 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,268,644 to Umehara et al. (hereinafter "Umehara") in view of U.S. Patent 6,265,762 to Tanaka et al. (hereinafter "Tanaka") and U.S. Patent 6,060,770 to Nakamura et al. (hereinafter "Nakamura"). This rejection is respectfully traversed.

The Umehara, Tanaka, and Nakamura references, whether taken alone or in combination, fail to teach or suggest a semiconductor chip having a plurality of dummy pads arranged on sides of the chip at positions free of I/O pads and spaced at the same pitch as the I/O pads, such that the chip is full of the plurality of equally spaced I/O pads and dummy pads.

With reference to FIG. 2 of Umehara, as cited in the Office Action, a chip 13 is mounted on a substrate 12, and peripherally-situated electrode pads 13a of the chip 13 are connected by wires 14 to stitch pads 12a on the substrate 12 (see column 4, lines 1-15). Between the wires 14a and 14b that are closest to corners of the chip 13, dummy wires 17 are connected to dummy electrode pads 16 on the chip 13 and dummy stitch pads 18 on the substrate 12, and the corners of the chip 13 "are inserted in between the wires" (i.e., dummy wires 17, as cited in Abstract). The dummy wires 17 suppress the flow of molding resin and prevent deformation of or contact between wires to reduce the risk of short circuits (see column 4, lines 61-65).

Umehara does not teach or suggest the arrangement of dummy pads as recited in claims 1, 6, and 10. For example, as shown in FIG. 2 of Umehara, the sides of the semiconductor chip 13 are not fully occupied by electrode pads 13a and dummy pads 16; in fact, FIG. 2 illustrates a gap between the two dummy pads 16 situated at the corner of the chip 13.

In contrast, the Applicants' claimed invention requires that the dummy pads occupy positions along the sides (including corners) of the semiconductor chip which are free of I/O pads, such that the sides of the semiconductor chip are full of equally spaced I/O pads and dummy pads. As discussed above, the claimed invention provides significant advantages over the prior art, i.e., encapsulation material will be more evenly distributed on the semiconductor chip during a subsequent potting process. Umehara fails to teach or suggest the claimed structure and resulting advantages of claims 1, 6, and 10.

The Tanaka reference relates to a semiconductor device in which inner leads 4 of a lead frame 1 are connected to a supporting body 8, a chip 10 is mounted on a chip mounting area 2, and the chip 10 is electrically connected to the inner leads 4 by wires 13 (see, e.g., FIG. 17, as cited in the Office Action). The pad pitch of pad electrodes 11 on the chip 10 is made wider near the corners, so as to prevent short circuiting if wires 13 at corner positions come into contact with adjacent wires 13 (see column 6, lines 58-65). As shown in FIG. 17, a dummy lead 20 is provided at a corner position and made wider than the inner leads 4, where the tip/point of the dummy lead 20 is spaced further outward than the tips/points of the inner leads 4 arranged on the periphery of the chip mounting area 2 (see column 9, lines 21-30).

Therefore, Tanaka teaches that the pad pitch of pad electrodes located at the corners of a semiconductor chip should be made wider than the pad pitch of other pad electrodes (see column 2, lines 63-65). Accordingly, the Tanaka reference, whether taken alone or in combination with Umehara, fails to teach or suggest a plurality of dummy pads arranged on sides of a semiconductor chip and which have the same pitch as I/O pads. Tanaka also fails to teach or suggest providing I/O pads and dummy pads such that the sides of the semiconductor chip are full of the equally spaced I/O pads and dummy pads.

With reference to FIG. 5 and FIG. 28 (i.e., "cover fig." cited in the Office Action), Nakamura relates to a semiconductor device in which a chip 2 is mounted in a device hole 8 of an insulating tape 4, the chip 2 being connected by inner leads 5a that are bonded to bonding pads 6a arranged on one side of the chip 2. Dummy pads 6b are arranged at respective corner portions of only one side of the chip, i.e., opposite to the side containing bonding pads 6a (see column 5, lines 61-64). Dummy leads 5 connected to the dummy pads 6b are used to support the chip 2 during potting of a resin onto the chip 2, thereby preventing the chip 2 from tilting due to the weight of the resin.

As shown in FIG. 28, for example, the dummy pads 6b are located at corners of the chip 2 opposite to the side having the bonding pads 6a, but are not arranged along all sides of the chip so as to fill the sides with I/O and dummy pads, as required in claims 1, 6, and 10. Moreover, the

dummy pads 6b situated at the corners do not have the same pitch as the bonding pads 6a, as required in the Applicants' claimed invention.

The Applicants' claimed invention requires dummy pads to be arranged at positions not occupied by I/O pads so as to fill the sides of the semiconductor chip with I/O and dummy pads having the same pitch, in order to facilitate even distribution of encapsulation material to prevent voids or popcorn effect. As shown in FIG. 28 of Nakamura, the corners of the side having the bonding pads 6a are not supported by any leads, and thus are subject to problems such as voids and popcorn effect, which are expressly avoided by the arrangement of I/O pads and bonding pads as recited in the Applicants' claimed invention. In Nakamura, the dummy leads 5 are simply used for mechanical support, but do not facilitate the even distribution of encapsulation material.

For at least the reasons discussed above, Nakamura could not be combined with Umehara and Tanaka to produce the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

Date: August 27, 2003

Peter F. Corless (Reg. No. 33,860)
Steven M. Jensen (Reg. No. 42,693)
Dike Bronstein, Roberts & Cushman
Intellectual Property Practice Group
EDWARDS & ANGELL, LLP
P.O. Box 9169
Boston, MA 02209

Phone: (617) 439-4444

Customer No. 21874